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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/680,963	10/06/2000	Tetsuo Yamada	P107317-00017	1445

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EXAMINER	
LONG, HEATHER R	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/680,963	YAMADA, TETSUO	
	Examiner	Art Unit	
	Heather R. Long	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *10-14* is/are withdrawn from consideration.

5)☒ Claim(s) *7-9* is/are allowed.

6)☒ Claim(s) *1-3 and 15-17* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2005 and 11 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-9 and 15-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-3 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Ishigami et al. (U.S. Patent 6,452,634).

Regarding claim **1**, the admitted prior art discloses in Figs. 15A and 15B a charge transfer device comprising: a semiconductor substrate (101); a charge transfer path formed in the semiconductor substrate and made of a first conductivity type semiconductor layer (105); and a plurality of charge transfer electrodes formed near above the charge transfer path (121). However, the prior art fails to teach a first pulse signal generator circuit for applying a either a first pulse signal train for n-phase (n being an integer larger than 1) driving of charges in the charge transfer path to the charge transfer electrodes or a second pulse signal train for (n + 1)-phase driving of charges in the charge transfer path to the charge transfer electrodes.

Referring to the Ishigami et al. reference, Ishigami et al. discloses in Fig. 17 a charge transfer device comprising a first pulse signal generator circuit for

applying either a first pulse signal train for n-phase (n being an integer larger than 1) driving of charges in the charge transfer path to the charge transfer electrodes or a second pulse signal train for (n + 1)-phase driving of charges in the charge transfer path to the charge transfer electrodes (paragraphs [0136]-[0139] and [0147]-[0149]: n-phase being 2 and (n + 1)-phase being 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teaching of using a first signal generator for applying a first or second pulse signal train to the charge transfer electrodes as taught by Ishigami et al. with the charge transfer device as disclosed by the admitted prior art in order to provide a charge transfer device which can reduce an output period without changing a drive frequency.

Regarding claim **2**, the admitted prior art discloses in Figs. 15A and 15B a charge transfer device comprising: a semiconductor substrate (101); a charge transfer path formed in the semiconductor substrate and made of a first conductivity type semiconductor layer (105); and a plurality of charge transfer electrodes formed near above the charge transfer path (121). However, the prior art fails to teach a second pulse signal generator circuit for applying either a first pulse signal train for n-phase driving (n being an integer larger than 1) of charges in the charge transfer path to the charge transfer electrodes or a third pulse signal train for (n x m)-phase driving (m being an integer larger than 1) of charges in the charge transfer path to the charge transfer electrodes.

Referring to the Ishigami et al. reference, Ishigami et al. discloses in Fig. 10 a charge transfer device comprising a second pulse signal generator circuit for applying either a first pulse signal train for n-phase driving (n being an integer larger than 1) of charges in the charge transfer path to the charge transfer electrodes or a third pulse signal train for (n x m)-phase driving (m being an integer larger than 1) of charges in the charge transfer path to the charge transfer electrodes (paragraphs [0077], [0078], [0083], and [0084]: n-phase being 2 and (n x m)-phase being 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teaching of Ishigami et al. with the charge transfer device of the admitted prior art in order to decrease power consumption and increase the maximum transfer quantity of signal charges.

Regarding claim **3**, the admitted prior art discloses in Figs. 15A and 15B a charge transfer device comprising: a semiconductor substrate (101); a charge transfer path formed in the semiconductor substrate and made of a first conductivity type semiconductor layer (105), the charge transfer path having first barrier layers having a high potential and first well layers having a low potential, disposed alternately (Fig. 15A, t1); a plurality of first and second charge transfer electrodes alternately formed near above the first barrier layers and first well layers of the charge transfer device (121 and Fig. 17); and a plurality of charge transfer electrode pairs each having adjacent first and second two charge

transfer electrodes connected together (Fig. 17). However, the prior art fails to disclose a third pulse signal generator circuit for applying either a fourth pulse signal train of two-phase for 2-phase driving of charges in the charge transfer path to two charge transfer electrode pairs or a fifth pulse signal train for 2k-pulse driving or more of charges in the charge transfer path to the charge transfer electrode pairs.

Referring to the Ishigami et al. reference, Ishigami et al. discloses a charge transfer device comprising a third pulse signal generator circuit for applying either a fourth pulse signal train of two-phase for 2-phase driving of charges in the charge transfer path to two charge transfer electrode pairs or a fifth pulse signal train for 2k-phase driving or more of charges in the charge transfer path to the charge transfer electrode pairs (paragraphs [0077], [0078], [0083], and [0084]; col. 8, lines 16-20: 2-phase being 2 and 2k-phase being 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teaching of Ishigami et al. with the charge transfer device of the admitted prior art in order to decrease power consumption and increase the maximum transfer quantity of signal charges.

Regarding claim **15**, the admitted prior art in view of Ishigami et al. discloses all the limitations as previously discussed with respect to claim 1 as well as Ishigami et al. further disclosing in Fig. 17 a charge transfer device wherein the charge transfer path is a horizontal charge transfer path and the first

pulse signal generator circuit applies either a first pulse signal train for n-phase (n being an integer larger than 1) driving of charges in the horizontal charge transfer path to the charge transfer electrodes or a second pulse signal train for (n + 1)-phase driving of charges in the horizontal charge transfer path to the charge transfer electrodes (paragraphs [0136]-[0139] and [0147]-[0149]: n-phase being 2 and (n + 1)-phase being 3).

Regarding claim **16**, the admitted prior art in view of Ishigami et al. discloses all the limitations as previously discussed with respect to claim 2 as well as Ishigami et al. further disclosing in Fig. 10 a charge transfer device wherein the charge transfer path is a horizontal charge transfer path and the second pulse signal generator circuit applies either a first pulse signal train for n-phase driving (n being an integer larger than 1) of charges in the horizontal charge transfer path to the charge transfer electrodes or a third pulse signal train for (n x m)-phase driving (m being an integer larger than 1) of charges in the horizontal charge transfer path to the charge transfer electrodes (paragraphs [0077], [0078], [0083], and [0084]: n-phase being 2 and (n x m)-phase being 4).

Regarding claim **17**, the admitted prior art in view of Ishigami et al. discloses all the limitations as previously discussed with respect to claim 3 as well as Ishigami et al. further disclosing a charge transfer device wherein the charge transfer path is a horizontal charge transfer path and the third pulse signal generator circuit applies either a fourth pulse signal train of two-phase for 2-phase driving of charges in the horizontal charge transfer path to two charge

transfer electrode pairs or a fifth pulse signal train for 2k-phase driving or more of charges in the horizontal charge transfer path to the charge transfer electrode pairs (paragraphs [0077], [0078], [0083], and [0084]; col. 8, lines 16-20: 2-phase being 2 and 2k-phase being 4).

Allowable Subject Matter

4. Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: prior art fails to fairly teach or suggest a charge transfer device, in combination with all the other elements claimed, a charge storage region formed adjacent to the final stage of the charge transfer electrodes for temporarily storing charges transferred in the charge transfer path; and a charge detection region for detecting an amount of charges stored in the charge storage region.

6. Claims 7-9 are allowed.

7. The following is an examiner's statement of reasons for allowance: prior art fails to fairly teach or suggest a charge transfer device, in combination with all the other elements claimed, a charge storage region formed adjacent to the final stage of the charge transfer electrodes for temporarily storing charges transferred in the charge transfer path; and a charge detection region for detecting an amount of charges stored in the charge storage region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather R. Long whose telephone number is 571-272-

7368. The examiner can normally be reached on Mon. - Thurs.: 7:00 am - 4:30 pm, and every other Fri.: 7:00 am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on 571-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Heather R Long
Examiner
Art Unit 2615

HRL
July 8, 2005

DAVID L. OMETZ
PRIMARY EXAMINER